IN THE CLAIMS:

Please amend the paragraph numbered [0085] in the originally-filed specification (numbered [0063] in the published patent application) as follows.

[0085] For design instance 620 design nodes are matched with pattern nodes in accordance with the method disclosed in this invention. It can be clearly seen that all nodes match and hence there is a pattern match. In contrast, the same process takes place for design instance 630. However, in this case the match fails at level 2, where a XOR gate is found as an input to the Flip-Flop. At this point the comparison will fail, in accordance with the method disclosed in this invention. According to an embodiment of the invention, it is possible to start pattern matching from each node in each pattern and comparing against each node in the design in turn. However, according to another embodiment, efficiency is gained by starting by comparing at likely correspondence points between the design and each pattern. According to yet another embodiment of the invention, correspondence points that are relatively rare in the design are chosen with a highest priority. Candidate correspondence points can be established for each pattern by looking for characteristics in the pattern that are known to be relatively rare in a typical design. For example, if the pattern contains a 32-bit adder, that 32-bit adder would be a suitable correspondence point, since 32-bit adders are relatively rare, for example in comparison to flip-flops, in most designs. Alternatively, considering the synchronizer example introduced earlier, a suitable correspondence point could be a crossing of clock domains, i.e., a flip-flop (FF) clocked by one clock but receiving data from an asynchronous clock domain. Such FFs are relatively rare in a typical design. Regardless of which are chosen, they will be referred to herein as "correspondence elements".

OK to Enter
09/26/2006
WMD